19-3539; Rev 1; 8/05

EVALUATION KIT AVAILABLE

Dual Step-Down DC-DC Power-Management ICs for Portable Devices

General Description

The MAX8621Y/MAX8621Z power-management integrated circuits (PMICs) are designed for a variety of portable devices including cellular handsets. These PMICs include two high-efficiency step-down DC-DC converters, four low-dropout linear regulators (LDOs) with pin-programmable capability, one open-drain driver, a 60ms (typ) reset timer, and power-on/off control logic. These devices offer high efficiency with a no-load supply current of 160µA, and their small thin QFN 4mm x 4mm package makes them ideal for portable devices.

The step-down DC-DC converters utilize a proprietary 4MHz hysteretic-PWM control scheme that allows for ultra-small external components. Internal synchronous rectification improves efficiency and eliminates the external Schottky diode that is required in conventional step-down converters. The output voltage is adjustable from 0.6V to 3.3V. The output current is guaranteed up to 500mA.

The four LDOs offer low 45µV_{RMS} output noise and low dropout of only 100mV at 100mA. OUT1 and OUT2 deliver 300mA (min) of continuous output current. OUT3 and OUT4 deliver 150mA (min) of continuous output current. The output voltages are pin selectable by SEL1 and SEL2 for flexibility. The MAX8621Y/MAX8621Z offer different sets of LDO output voltages.

A microprocessor reset output ($\overline{RESET}$) monitors OUT1 and warns the system of impending power loss, allowing safe shutdown. $\overline{RESET}$ asserts during power-up, power-down, shutdown, and fault conditions where V_{OUT1} is below its regulation voltage.

A 200mA driver output is provided to control LED backlighting or provide an open-drain connection for resistors such as in feedback networks.

Applications

Cellular Handsets

Smart Phones, PDAs

Digital Cameras

MP3 Players

Wireless LAN

Pin Configuration appears at end of data sheet.

Features

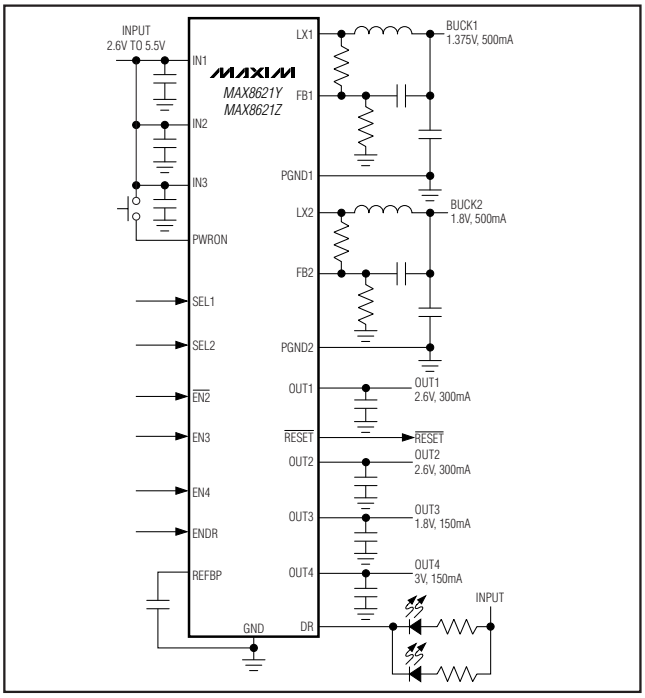
- **Two 500mA Step-Down Converters**
  Up to 4MHz Switching Frequency
  Adjustable Output from 0.6V to 3.3V
- **Four Low-Noise LDOs with Pin-Programmable Output Voltages**
- **One Open-Drain Driver**
- **60ms (typ) Reset Timer**
- **Power-On/Off Control Logic and Sequencing**
- **4mm x 4mm x 0.8mm 24-Pin Thin QFN**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX8621YETG	-40°C to +85°C	24 Thin QFN 4mm x 4mm (T2444-4)
MAX8621YETG+	-40°C to +85°C	24 Thin QFN 4mm x 4mm (T2444-4)
MAX8621ZETG	-40°C to +85°C	24 Thin QFN 4mm x 4mm (T2444-4)
MAX8621ZETG+	-40°C to +85°C	24 Thin QFN 4mm x 4mm (T2444-4)

+ Denotes lead-free package.

Typical Operating Circuit



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ABSOLUTE MAXIMUM RATINGS

PWRON, IN1, IN2, IN3, $\overline{RESET}$, FB1, FB2, ENDR, REFBP, SEL1, SEL2 to GND .....-0.3V to +6.0V
$\overline{EN2}$, EN3, EN4, DR to GND .....-0.3V to (V_{IN3} + 0.3V)
OUT1, OUT2, OUT3, OUT4 to GND .....-0.3V to (V_{IN2} + 0.3V)
PGND1, PGND2 to GND .....-0.3V to + 0.3V
LX1, LX2 Current .....±1.5A_{RMS}
LX1, LX2 to GND (Note 1) .....-0.3V to (V_{IN1} + 0.3V)
DR Current .....0.5A_{RMS}

Continuous Power Dissipation (T_A = +70°C)
24-Pin 4mm x 4mm Thin QFN
(derate 27.8mW/°C above +70°C) 2222.2mW
Operating Temperature Range .....-40°C to +85°C
Junction Temperature .....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Note 1: LX_ has internal clamp diodes to GND and IN1. Applications that forward-bias these diodes should take care not to exceed the IC's package dissipation limits.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{IN} = 3.7V, C_{IN1} = 10µF, C_{IN2} = C_{IN3} = 4.7µF, C_{OUT1} = C_{OUT2} = 4.7µF, C_{OUT3} = C_{OUT4} = 2.2µF, C_{REFBP} = 0.01µF, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Notes 1, 2)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Input Supply Range	After startup	2.6		5.5	V
Shutdown Supply Current	V_{IN} = 4.2V (Note 3)		2	15	µA
No-Load Supply Current	V_{IN} = 3.7V; BUCK1, BUCK2, OUT1, OUT2 on; other circuits off		160	300	µA
	V_{IN} = 3.7V, BUCK1 and BUCK2 on, all LDOs on		275		
Light-Load Supply Current	V_{IN} = 3.7V, BUCK1 and BUCK2 with 500µA load each, OUT1 and OUT2 on, other circuits off		710		µA
UNDERVOLTAGE LOCKOUT					
Undervoltage Lockout (Note 4)	V_{IN} rising	2.70	2.85	3.05	V
	V_{IN} falling		2.35	2.55	
THERMAL SHUTDOWN					
Threshold	T_A rising		+160		°C
Hysteresis			15		°C
REFERENCE					
Reference Bypass Output Voltage	T_A = 0°C to +85°C	1.235	1.250	1.265	V
REF Supply Rejection	2.6V ≤ V_{IN} ≤ 5.5V		0.2		mV/V
LOGIC AND CONTROL INPUTS					
Input Low Level	PWRON, $\overline{EN2}$, EN3, EN4; 2.6V ≤ V_{IN} ≤ 5.5V			0.4	V
Input High Level	PWRON, $\overline{EN2}$, EN3, EN4; 2.6V ≤ V_{IN} ≤ 4.2V	1.44	1.12		V
	PWRON, $\overline{EN2}$, EN3, EN4; 2.6V ≤ V_{IN} ≤ 5.5V		1.25		
Logic Input Current	EN3, EN4; 0V < V_{IN} < 5.5V	-1		+1	µA
Tristate Low Input Threshold	SEL_	0.3	0.7	1.0	V
Tristate Low Input Threshold Hysteresis	SEL_		50		mV
Tristate High Input Threshold	SEL_	V_{IN} - 1.2V	V_{IN} - 0.8V	V_{IN} - 0.4V	V

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = 3.7V, C_{IN1} = 10µF, C_{IN2} = C_{IN3} = 4.7µF, C_{OUT1} = C_{OUT2} = 4.7µF, C_{OUT3} = C_{OUT4} = 2.2µF, C_{REFBP} = 0.01µF, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Notes 1, 2)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Tristate High Input Threshold Hysteresis	SEL_		50		mV
PWRON, $\overline{EN2}$ Pulldown Resistor to GND		400	800	1600	kΩ
STEP-DOWN DC-DC CONVERTER 1 (BUCK1)					
Supply Current	I_{LOAD} = 0A, no switching		40		µA
Output Voltage Range		0.6		3.3	V
FB1 Threshold Voltage	V_{FB1} falling		0.603		V
FB1 Threshold Line Regulation	2.6V ≤ V_{IN} ≤ 5.5V		0.3		%/V
FB1 Threshold Voltage Hysteresis (% of V_{FB1})			1		%
FB1 Bias Current	Shutdown		0.01		µA
	V_{FB1} = 0.5V		0.01		
Current Limit	p-MOSFET switch (I_{LIMP})	670	1000	1500	mA
	n-MOSFET rectifier (I_{LIMN})	750	1000	1330	
On-Resistance	p-MOSFET switch, I_{LX1} = -40mA		0.65	1.5	Ω
	n-MOSFET rectifier, I_{LX1} = 40mA		0.35	0.8	
Rectifier Off-Current Threshold	I_{LXOFF}		45	70	mA
Minimum On- and Off-Times	t_{ON}		107		ns
	t_{OFF}		95		
STEP-DOWN DC-DC CONVERTER 2 (BUCK2)					
Supply Current	I_{LOAD} = 0A, no switching		40		µA
Output Voltage Range		0.6		3.3	V
FB2 Threshold Voltage	V_{FB2} falling		0.603		V
FB2 Threshold Line Regulation	2.6V ≤ V_{IN} ≤ 5.5V		0.3		%/V
FB2 Threshold Voltage Accuracy (Falling) (% of VFB2)	I_{LOAD} = 0A	-2.5		+2.5	%
FB2 Threshold Voltage Hysteresis (% of VFB2)			1		%
FB2 Bias Current	Shutdown		0.01		µA
	V_{FB} = 0.5V		0.01		
Current Limit	p-MOSFET switch	670	1000	1500	mA
	n-MOSFET rectifier	750	1000	1330	
On-Resistance	p-MOSFET switch, I_{LX2} = -40mA		0.65	1.5	Ω
	n-MOSFET rectifier, I_{LX2} = 40mA		0.35	0.8	
Rectifier Off-Current Threshold	I_{LXOFF}		45	70	mA
Minimum On- and Off-Times	t_{ON}		107		ns
	t_{OFF}		95		

Dual Step-Down DC-DC Power-Management ICs for Portable Devices

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = 3.7V, C_{IN1} = 10µF, C_{IN2} = C_{IN3} = 4.7µF, C_{OUT1} = C_{OUT2} = 4.7µF, C_{OUT3} = C_{OUT4} = 2.2µF, C_{REFBP} = 0.01µF, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Notes 1, 2)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNIT
OUT1 (LDO1)						
Output Voltage Accuracy	I_{LOAD} = 1mA, 3.7V ≤ V_{IN} ≤ 5.5V, relative to $V_{OUT(NOM)}$	T_A = 0°C to +85°C	-1.3	+0.6	+2.0	%
		T_A = -40°C to +85°C	-2.3		+2.5	
	I_{LOAD} = 150mA, relative to $V_{OUT(NOM)}$			0		
Output Current					300	mA
Current Limit	V_{OUT1} = 0V		310	550	940	mA
Dropout Voltage	I_{LOAD} = 200mA, T_A = +85°C			200	420	mV
Load Regulation	V_{IN} = greater of 3.7V or ($V_{OUT(NOM)}$ + 0.7V), 1mA < I_{LOAD} < 300mA, V_{SEL1} = V_{SEL2} = 0V			1.2		%
Power-Supply Rejection $\Delta V_{OUT1}/\Delta V_{IN2}$	10Hz to 10kHz, C_{OUT1} = 4.7µF, I_{LOAD} = 30mA			60		dB
Output Noise Voltage (RMS)	100Hz to 100kHz, C_{OUT1} = 4.7µF, I_{LOAD} = 30mA			45		μV_{RMS}
Output Capacitor for Stable Operation	0 < I_{LOAD} < 300mA			4.7		µF
	0 < I_{LOAD} < 150mA			2.2		
Ground Current	I_{LOAD} = 500µA			21		µA
OUT2 (LDO2)						
Output Voltage Accuracy	I_{LOAD} = 1mA, 3.7V ≤ $V_{IN\_}$ ≤ 5.5V, relative to $V_{OUT(NOM)}$	T_A = 0°C to +85°C	-1.3	+0.6	+2.0	%
		T_A = -40°C to +85°C	-2.3		+2.5	
	I_{LOAD} = 150mA, relative to $V_{OUT(NOM)}$			0		
Output Current					300	mA
Current Limit	V_{OUT2} = 0V		310	550	940	mA
Dropout Voltage	I_{LOAD} = 200mA , T_A = +85°C			200	420	mV
Load Regulation	1mA < I_{LOAD} < 300mA, V_{SEL1} = V_{SEL2} = 0V			1.2		%
Power-Supply Rejection $\Delta V_{OUT2}/\Delta V_{IN2}$	10Hz to 10kHz, C_{OUT2} = 4.7µF, I_{LOAD} = 30mA			60		dB
Output Noise Voltage (RMS)	100Hz to 100kHz, C_{OUT2} = 4.7µF, I_{LOAD} = 30mA			45		μV_{RMS}
Output Capacitor for Stable Operation	0 < I_{LOAD} < 300mA			4.7		µF
	0 < I_{LOAD} < 150mA			2.2		
Ground Current	I_{LOAD} = 500µA			21		µA
OUT3 (LDO3)						
Output Voltage Accuracy	I_{LOAD} = 1mA, 3.7V ≤ $V_{IN\_}$ ≤ 5.5V, relative to $V_{OUT(NOM)}$	T_A = 0°C to +85°C	-1.3	+0.3	+2.0	%
		T_A = -40°C to +85°C	-2.3		+2.5	
	I_{LOAD} = 75mA, relative to $V_{OUT(NOM)}$			0		
Output Current					150	mA
Current Limit	V_{OUT3} = 0V		165	360	650	mA
Dropout Voltage	I_{LOAD} = 100mA , T_A = +85°C			100	210	mV
Load Regulation	1mA < I_{LOAD} < 150mA, V_{SEL1} = V_{SEL2} = 0V			0.6		%

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = 3.7V, C_{IN1} = 10µF, C_{IN2} = C_{IN3} = 4.7µF, C_{OUT1} = C_{OUT2} = 4.7µF, C_{OUT3} = C_{OUT4} = 2.2µF, C_{REFBP} = 0.01µF, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Notes 1, 2)

PARAMETER	CONDITIONS			MIN	TYP	MAX	UNIT
Power-Supply Rejection $\Delta V_{OUT3}/\Delta V_{IN2}$	10Hz to 10kHz, C_{OUT3} = 2.2µF, I_{LOAD} = 30mA				60		dB
Output Noise Voltage (RMS)	100Hz to 100kHz, C_{OUT3} = 2.2µF, I_{LOAD} = 30mA				45		μV_{RMS}
Output Capacitor for Stable Operation	0 < I_{LOAD} < 150mA				2.2		µF
OUT4 (LDO4)							
Output Voltage Accuracy	I_{LOAD} = 1mA, 3.7V ≤ $V_{IN\_}$ ≤ 5.5V, relative to $V_{OUT(NOM)}$	T_A = 0°C to +85°C	$V_{OUT(NOM)}$ ≥ 1.8V	-1.3	+0.3	+2.0	%
			$V_{OUT(NOM)}$ = 1.5V	-1.30	+0.3	+2.35	
		T_A = -40°C to +85°C		-2.3		+2.5	
	I_{LOAD} = 75mA, relative to $V_{OUT(NOM)}$				0		
Output Current						150	mA
Current Limit	V_{OUT4} = 0V			165	360	650	mA
Dropout Voltage	I_{LOAD} = 100mA, T_A = +85°C				100	210	mV
Load Regulation	1mA < I_{LOAD} < 150mA, V_{SEL1} = V_{SEL2} = 0				0.6		%
Power-Supply Rejection $\Delta V_{OUT4}/\Delta V_{IN2}$	10Hz to 10kHz, C_{OUT4} = 2.2µF, I_{LOAD} = 30mA				60		dB
Output Noise Voltage (RMS)	100Hz to 100kHz, C_{OUT4} = 2.2µF, I_{LOAD} = 30mA				45		μV_{RMS}
Output Capacitor for Stable Operation	0 < I_{LOAD} < 150mA				2.2		µF
DRIVER (DR)							
ENDR Turn-On Threshold	I_{DR} = 1mA				0.65		V
ENDR Input Current	V_{ENDR} = 0V and 5.5V			-1		+1	µA
DR Output Low Voltage	I_{DR} = 150mA, V_{ENDR} = 3.7V				0.2	0.4	V
DR Off-Current (Leakage)	V_{DR} = V_{IN} = 5.5V, V_{ENDR} = 0V			-1		+1	µA
$\overline{\text{RESET}}$							
Output High Voltage				V_{OUT1} - 0.3V			V
Output Low Voltage	I_{SINK} = 1mA					0.3	V
$\overline{\text{RESET}}$ Threshold	Percentage of nominal OUT1 rising when $\overline{\text{RESET}}$ falls			84	87	90	%
$\overline{\text{RESET}}$ Active Timeout Period	From OUT1 ≥ 87% until $\overline{\text{RESET}}$ = HIGH				60		ms
Pullup Resistance to OUT1				8	14	20	kΩ

Note 1: V_{IN1}, V_{IN2}, and V_{IN3} are shorted together and single input is referred to as V_{IN}.
Note 2: All units are 100% production tested at T_A = +85°C. Limits over the operating range are guaranteed by design.
Note 3: OUT1, OUT2, OUT3, OUT4, LX1, and LX2 to ground.
Note 4: When the input voltage is greater than 2.85V (typ), the UVLO comparator trips and the threshold is reduced to 2.35V (typ). This allows the system to start normally until the input voltage decays to 2.35V.

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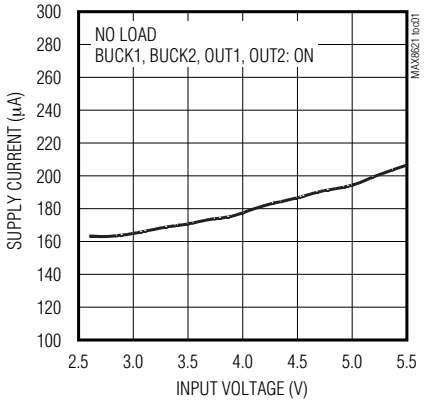
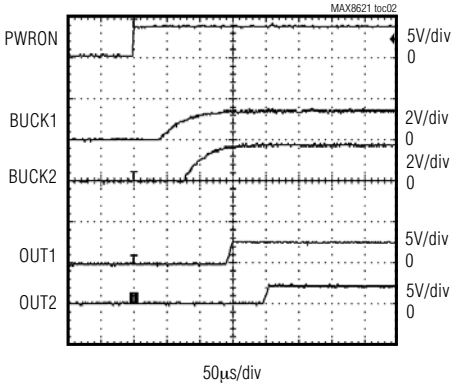
Typical Operating Characteristics

(Circuit of Figure 3, $V_{IN1} = V_{IN2} = V_{IN3} = 3.6V$, PWRON = IN, $V_{BUCK1} = 1.375V$, $V_{BUCK2} = 1.8V$, $V_{OUT1} = 2.6V$, $V_{OUT2} = 2.6V$, $V_{OUT3} = 1.8V$, $V_{OUT4} = 3.0V$, SEL1 = SEL2 = open, LX1 = LX2 = Murata LQH32CN2R2M53, $T_A = +25°C$, unless otherwise noted.)

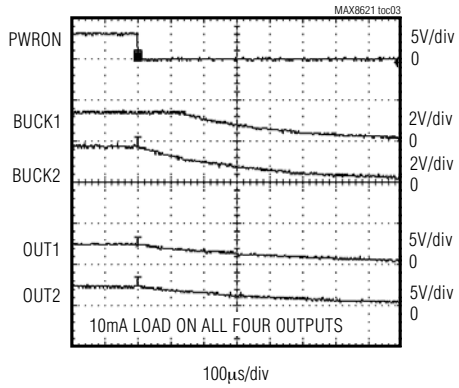
SUPPLY CURRENT vs. INPUT VOLTAGE



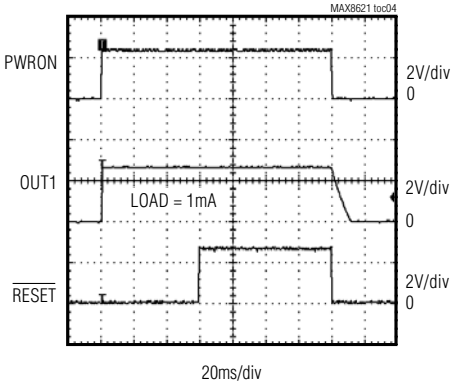
STARTUP WAVEFORMS



SHUTDOWN WAVEFORMS



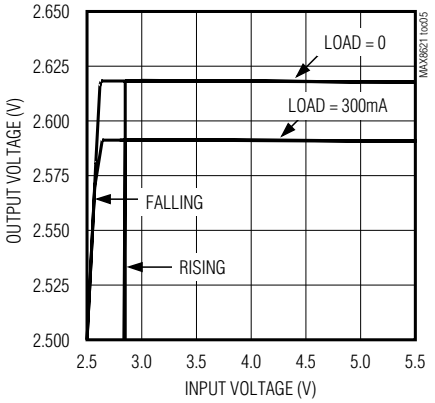
$\overline{\text{RESET}}$ WAVEFORMS



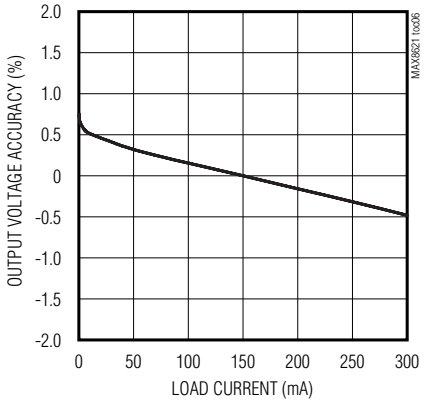
Typical Operating Characteristics (continued)

(Circuit of Figure 3, $V_{IN1} = V_{IN2} = V_{IN3} = 3.6V$, PWRON = IN, $V_{BUCK1} = 1.375V$, $V_{BUCK2} = 1.8V$, $V_{OUT1} = 2.6V$, $V_{OUT2} = 2.6V$, $V_{OUT3} = 1.8V$, $V_{OUT4} = 3.0V$, SEL1 = SEL2 = open, LX1 = LX2 = Murata LQH32CN2R2M53, $T_A = +25°C$, unless otherwise noted.)

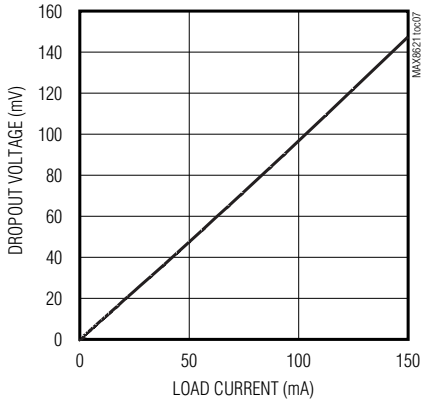
OUT1 OUPUT VOLTAGE vs. INPUT VOLTAGE



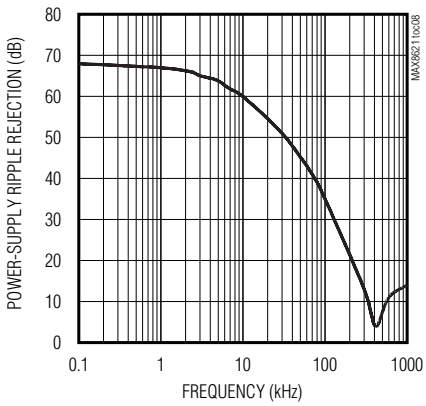
OUT2 OUTPUT VOLTAGE ACCURACY vs. LOAD CURRENT



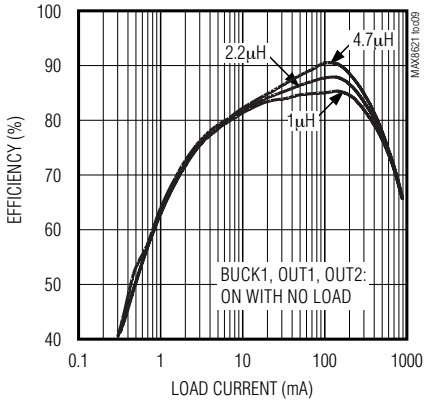
OUT4 DROPOUT VOLTAGE vs. LOAD CURRENT



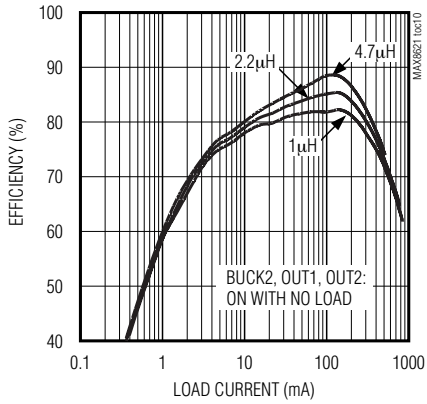
OUT1 POWER-SUPPLY RIPPLE REJECTION vs. FREQUENCY



EFFICICENCY vs. LOAD CURRENT ($V_{BUCK2} = 1.8V$)



EFFICICENCY vs. LOAD CURRENT ($V_{BUCK1} = 1.375V$)

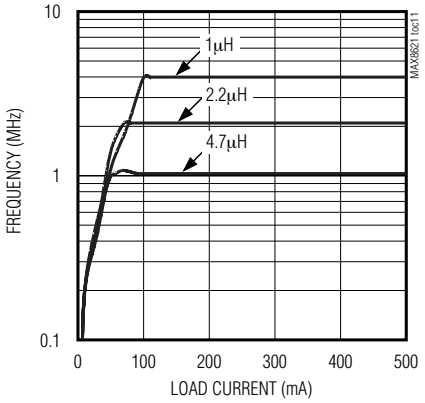


Dual Step-Down DC-DC Power-Management ICs for Portable Devices

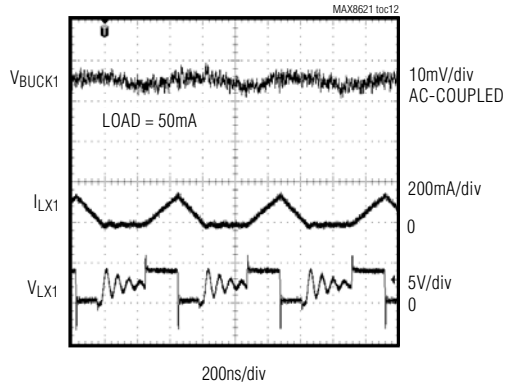
Typical Operating Characteristics (continued)

(Circuit of Figure 3, $V_{IN1} = V_{IN2} = V_{IN3} = 3.6V$, PWRON = IN, $V_{BUCK1} = 1.375V$, $V_{BUCK2} = 1.8V$, $V_{OUT1} = 2.6V$, $V_{OUT2} = 2.6V$, $V_{OUT3} = 1.8V$, $V_{OUT4} = 3.0V$, SEL1 = SEL2 = open, LX1 = LX2 = Murata LQH32CN2R2M53, $T_A = +25°C$, unless otherwise noted.)

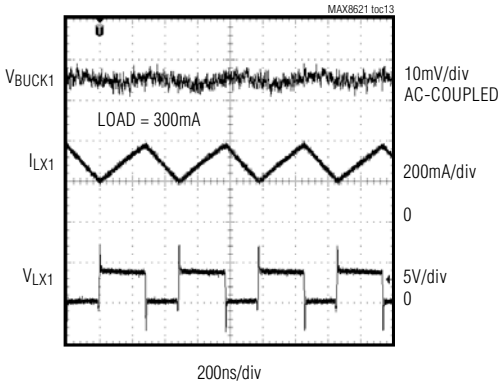
SWITCHING FREQUENCY vs. LOAD CURRENT



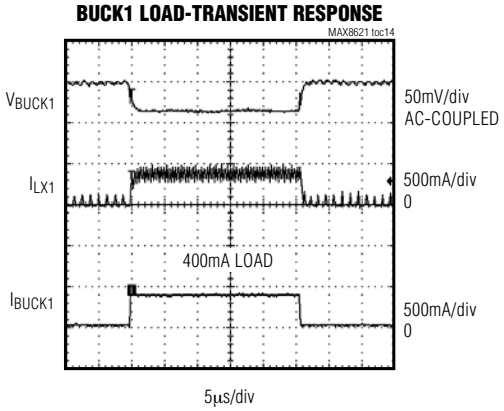
BUCK1 LIGHT-LOAD WAVEFORMS



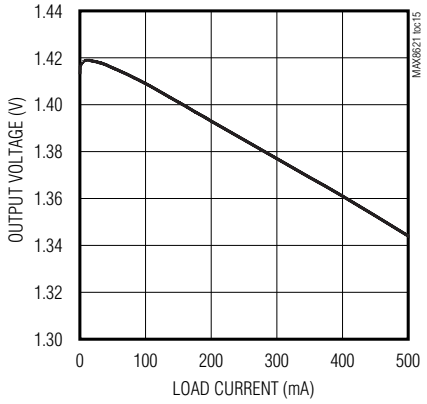
BUCK1 HEAVY-LOAD WAVEFORMS



BUCK1 LOAD-TRANSIENT RESPONSE



BUCK1 OUTPUT VOLTAGE vs. LOAD CURRENT (VOLTAGE POSITIONING)



Pin Description

PIN	NAME	FUNCTION
1	FB1	Voltage Feedback for Step-Down Converter 1. FB1 regulates to 0.6V nominal.
2	FB2	Voltage Feedback for Step-Down Converter 2. FB2 regulates to 0.6V nominal.
3	GND	Ground. Ground for all LDOs and the control section.
4	REFBP	Reference Noise Bypass. Connect a 0.01µF ceramic capacitor from REFBP to GND. Not intended to drive resistive load. REFBP is high impedance in shutdown.
5	EN4	Enable Input for OUT4. Drive EN4 high to turn on OUT4.
6	OUT4	150mA LDO4 output. Bypass OUT4 to GND with a 2.2µF ceramic capacitor. OUT4 is high impedance when disabled. OUT4 can only be activated if OUT1 is within 87% of regulation.
7	EN3	Enable Input for OUT3. Drive EN3 high to turn on OUT3.
8	$\overline{EN2}$	Enable Input for OUT2. Drive $\overline{EN2}$ high to disable OUT2. Drive $\overline{EN2}$ low or leave open to enable OUT2. $\overline{EN2}$ is internally pulled to GND by an 800kΩ (typ) pulldown resistor. If the MAX8621Y/MAX8621Z are placed into shutdown using PWRON (PWRON = low), OUT2 does not power regardless of the status of $\overline{EN2}$.
9	OUT2	300mA LDO2 Output. Bypass with a 4.7µF ceramic capacitor to GND. OUT2 is high impedance when disabled. OUT2 can only be activated if OUT1 is within 87% of regulation.
10	IN2	Supply Voltage to the Output MOSFET of All 4 LDOs. IN2 must be shorted to IN1 and IN3. Connect a 4.7µF ceramic capacitor from IN2 to GND.
11	$\overline{RESET}$	Open-Drain, Active-Low Reset Output. $\overline{RESET}$ asserts low when V_{OUT1} drops below 87% (typ) of regulation. $\overline{RESET}$ deasserts 60ms after V_{OUT1} rises above 87% (typ) of regulation (Figure 2).
12	OUT1	300mA LDO1 Output. Bypass with a 4.7µF ceramic capacitor to GND. OUT1 is high impedance when disabled.
13	OUT3	150mA LDO3 Output. Bypass OUT3 to GND with a 2.2µF ceramic capacitor. OUT3 is high impedance when disabled. OUT3 can only be activated if OUT1 is within 87% of regulation.
14	PWRON	Power Enable Input. Drive PWRON high to enable the MAX8621Y/MAX8621Z. Drive PWRON low to enter shutdown mode. PWRON has an internal 800kΩ (typ) pulldown resistor.
15	ENDR	Enable Input for DR. Drive ENDR low for DR to go into high impedance. Drive ENDR high to activate DR, pulling DR low.
16	IN3	Supply Voltage to the Control Section. IN3 must be shorted to IN1 and IN2. Connect a 4.7µF ceramic capacitor from IN3 to GND.
17	SEL2	LDO Output-Voltage Select Input 2. SEL1 and SEL2 set the OUT1, OUT2, OUT3, and OUT4 voltages to one of nine combinations (Table 1).
18	SEL1	LDO Output-Voltage Select Input 1. SEL1 and SEL2 set the OUT1, OUT2, OUT3, and OUT4 voltages to one of nine combinations (Table 1).
19	DR	200mA Driver Output. Connects to the open drain of an internal n-channel MOSFET whose gate is controlled by ENDR.
20	PGND2	Power Ground for BUCK2 and DR Switch
21	LX2	Inductor Connection for BUCK2. LX2 is internally connected to the drain of the internal p-channel MOSFET and the drain of the internal n-channel synchronous rectifier for BUCK2. LX2 is high impedance when BUCK2 is disabled.
22	IN1	Supply Voltage to the Output Stage of BUCK1 and BUCK2. IN1 must be shorted to IN2 and IN3. Connect a 10µF ceramic capacitor from IN1 to GND.
23	LX1	Inductor Connection for BUCK1. LX1 is internally connected to the drain of the internal p-channel MOSFET and the drain of the internal n-channel synchronous rectifier for BUCK1. LX1 is high impedance when BUCK1 is disabled.
24	PGND1	Power Ground for BUCK1
—	EP	Exposed Paddle. Connect the exposed paddle to GND, PGND1, and PGND2.

Dual Step-Down DC-DC Power-Management ICs for Portable Devices

Detailed Description

The MAX8621Y/MAX8621Z power-management ICs are designed specifically to power a variety of portable devices including cellular handsets. Each device contains two 4MHz high-efficient step-down converters, four low-dropout linear regulators (LDOs), a 60ms (typ) reset timer, a 200mA open-drain output driver, and power-on/off control logic (Figure 3).

Step Down DC-DC Control Scheme

The MAX8621Y/MAX8621Z step-down converters are optimized for high-efficiency voltage conversion over a wide load range, while maintaining excellent transient response, minimizing external component size, and minimizing output voltage ripple. The DC-DC converters (BUCK1 and BUCK2) also feature an optimized on-resistance internal MOSFET switch and synchronous rectifier to maximize efficiency. The MAX8621Y/MAX8621Z utilize a proprietary hysteretic-PWM control scheme that switches with nearly fixed frequency up to 4MHz, allowing for ultra-small external components. The step-down converter output current is guaranteed up to 500mA, while consuming 40µA (typ).

When the step-down converter output voltage falls below the regulation threshold, the error comparator begins a switching cycle by turning the high-side p-channel MOSFET switch on. This switch remains on until the minimum on-time (t_{ON}) expires and the output voltage is in regulation or the current-limit threshold (I_{LIMP}) is exceeded. Once off, the high-side switch remains off until the minimum off-time (t_{OFF}) expires and the output voltage again falls below the regulation threshold. During this off period, the low-side synchronous rectifier turns on and remains on until either the high-side switch turns on or the inductor current reduces to the rectifier-off current threshold (I_{LXOFF} = 45mA (typ)). The internal synchronous rectifier eliminates the need for an external Schottky diode.

Voltage-Positioning Load Regulation

The MAX8621Y/MAX8621Z use a unique step-down converter feedback network. By taking feedback from the LX node through R1, the usual phase lag due to the output capacitor is removed, making the loop exceedingly stable and allowing the use of a very small ceramic output capacitor. This configuration causes the output voltage to shift by the inductor series resistance multiplied by the load current. This output voltage shift is known as voltage-positioning load regulation. Voltage-positioning load regulation greatly reduces overshoot during load transients, which effectively halves the peak-to-peak output-voltage excursions compared to traditional step-down converters. See the Buck1 Load-Transient Response graph in the *Typical Operating Characteristics*.

Low-Dropout Linear Regulators

Each MAX8621Y/MAX8621Z contains four low-dropout, low-quiescent-current, high-accuracy linear regulators (LDOs). OUT1 and OUT2 supply loads up to 300mA, while OUT3 and OUT4 supply loads up to 150mA. The LDO output voltages are set using SEL1 and SEL2 (see Table 1). The LDOs include an internal reference, error amplifier, p-channel pass transistor, internal programmable voltage-divider, and an OUT1 power-good comparator. Each error amplifier compares the reference voltage to a feedback voltage and amplifies the difference. If the feedback voltage is lower than the reference voltage, the pass-transistor gate is pulled lower, allowing more current to pass to the outputs and increasing the output voltage. If the feedback voltage is too high, the pass-transistor gate is pulled up, allowing less current to pass to the output.

DR Driver

Each MAX8621Y/MAX8621Z includes a 1.3Ω n-channel MOSFET open-drain output that is controlled by ENDR. This output can be used to drive LEDs (see the *Typical Operating Circuit*) and allow adjustable output voltages (see Figure 1).

Programming LDO Output Voltages (SEL1, SEL2)

As shown in Table 1, the LDO output voltages, OUT1, OUT2, OUT3, and OUT4 are pin-programmable by the logic states of SEL1 and SEL2. SEL1 and SEL2 are trilevel inputs: IN, open, and GND. The input voltage, V_{IN}, must be greater than the selected OUT1, OUT2, OUT3, and OUT4 voltages. The logic states of SEL1 and SEL2 can be programmed only during power-up. Once the OUT_ voltages are programmed, their values do not change by changing SEL_ unless the MAX8621Y/MAX8621Z power is cycled.

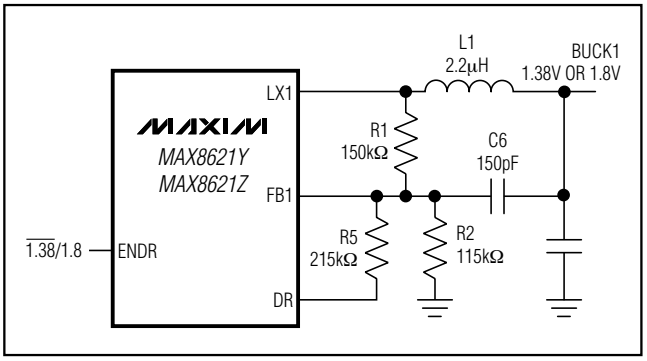


Figure 1. Adjusting BUCK1 Output Voltage Using DR

Table 1. SEL1 and SEL2, MAX8621Y/MAX8621Z Output Voltage Selection

SEL1	SEL2	MAX8621Y				MAX8621Z			
		OUT1 (V)	OUT2 (V)	OUT3 (V)	OUT4 (V)	OUT1 (V)	OUT2 (V)	OUT3 (V)	OUT4 (V)
IN	IN	3.3	3.3	2.85	2.85	2.8	2.6	3.0	3.0
IN	OPEN	3.0	3.3	3.3	2.85	2.6	2.6	3.0	3.0
IN	GND	2.5	3.3	2.85	3.0	2.6	2.6	2.9	2.9
OPEN	IN	2.85	3.3	3.0	2.5	2.6	2.6	3.0	3.3
OPEN	OPEN	3.3	3.3	2.8	3.0	2.6	2.6	1.8	3.0
OPEN	GND	3.3	3.3	3.0	3.0	2.6	2.6	2.8	3.0
GND	IN	3.3	2.85	3.3	2.85	2.9	3.1	1.8	1.5
GND	OPEN	2.85	2.85	3.3	3.3	3.0	2.9	2.9	2.9
GND	GND	3.3	2.85	3.0	3.0	3.0	2.5	2.9	2.9

Power-Supply Sequence

BUCK1 is always first on and last off in the MAX8621Y/MAX8621Zs' power sequence. BUCK1 turns on approximately 40µs after PWRON is enabled. BUCK2 turns on approximately 40µs after BUCK1, and OUT1 turns on 65µs after BUCK2. These delays have been added to sequence the turn-on of the step-down converters and LDOs so that the initial current surges are distributed over time. For the same reason, OUT2, OUT3, and OUT4 can be turned on by $\overline{EN2}$, EN3, and EN4 signals, but only after OUT1 has reached 87% of its final value. Note that OUT2 typically requires a longer time to enable than OUT3 and OUT4 (45µs versus 15µs). All regulators can be turned off at the same time when PWRON is low, but BUCK1 remains on for approximately another 120µs after PWRON goes low.

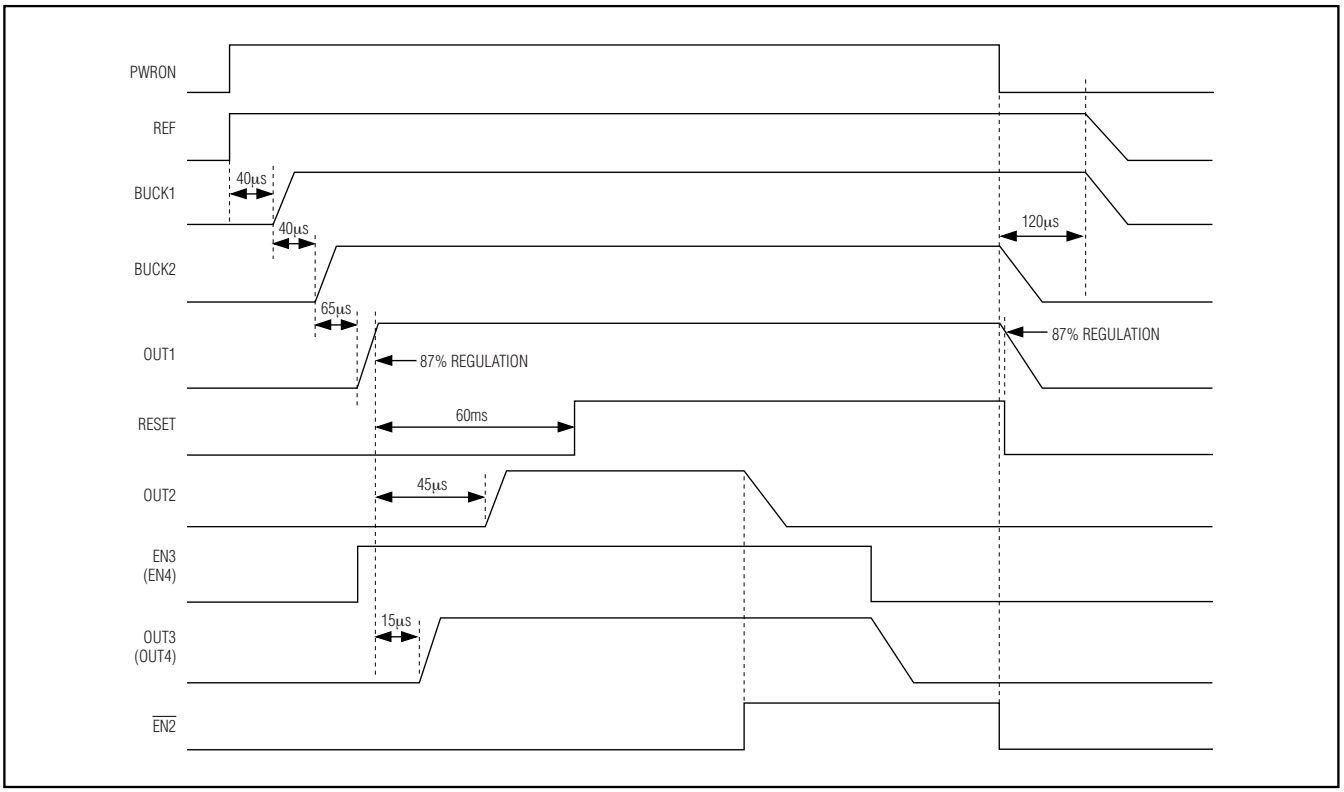


Figure 2. Power-On/Off Sequence Diagram

Dual Step-Down DC-DC Power-Management ICs for Portable Devices

PWRON

Drive PWRON low or leave PWRON open to place the MAX8621Y/MAX8621Z in power-down mode and reduce supply current to 5µA (typ). In power-down, the control circuitry, internal-switching p-channel MOSFET, and the internal synchronous rectifier (n-channel MOSFET) turn off (BUCK1 and BUCK2), and LX_ becomes high impedance. In addition, all four LDOs are disabled. Connect PWRON to IN or logic-high to enable the MAX8621Y/MAX8621Z. $\overline{EN2}$ enables and disables OUT2 when PWRON is high.

OUT2 Enable ($\overline{EN2}$)

Drive $\overline{EN2}$ high to disable OUT2. Drive $\overline{EN2}$ low or leave open to enable OUT2. $\overline{EN2}$ is internally pulled to GND by an 800kΩ (typ) pulldown resistor. If the MAX8621Y/MAX8621Z are powered down using PWRON (PWRON = low), OUT2 does not power regardless of the status of $\overline{EN2}$.

Reset Output ($\overline{RESET}$)

The reset circuit is active both at power-up and power-down. $\overline{RESET}$ asserts low when V_{OUT1} drops below 87% (typ) of regulation. $\overline{RESET}$ deasserts 60ms after V_{OUT1} rises above 87% (typ) of regulation. $\overline{RESET}$ is pulled up through an internal 14kΩ resistor to OUT1.

Undervoltage Lockout

Initial power-up of the MAX8621Y/MAX8621Z occurs when V_{IN} is greater than 2.85V (typ) and PWRON asserts. Once V_{IN} exceeds 2.85V (typ), the undervoltage lockout has 0.5V of hysteresis, allowing the V_{IN} operating range to drop down to 2.35V (typ) without shutting down.

Current Limiting

The MAX8621Y/MAX8621Z OUT1 and OUT2 LDOs limit their output current to 550mA (typ). OUT3 and OUT4 LDOs limit their output current to 360mA (typ). If the LDO output current exceeds the current limit, the corresponding LDO output voltage drops. The step-down converters (BUCK1 and BUCK2) limit the p-channel MOSFET to 670mA (min) and the n-channel MOSFET to 750mA (min).

Reference Bypass Capacitor Node (REFBP)

An external 0.01µF bypass capacitor and an internal 100kΩ (typ) resistor at REFBP create a lowpass filter for LDO noise reduction. OUT1, OUT2, OUT3, and OUT4 exhibit 45μV_{RMS} of output voltage noise with C_{REFBP} = 0.01µF, C_{OUT1} = C_{OUT2} = 4.7µF, and C_{OUT3} = C_{OUT4} = 2.2µF.

Thermal-Overload Protection

Thermal-overload protection limits total power dissipation in the MAX8621Y/MAX8621Z. Independent thermal-protection circuits monitor the step-down converters and the linear-regulator circuits. When the junction temperature exceeds T_J = +160°C, the thermal-overload protection circuit disables the corresponding circuitry, allowing the IC to cool. The LDO thermal-overload protection circuit enables the LDOs after the LDO junction temperature cools down, resulting in pulsed LDO outputs during continuous thermal-overload conditions. The step-down converter's thermal-overload protection circuitry enables the step-down converter after the junction temperature cools down. Thermal-overload protection safeguards the MAX8621Y/MAX8621Z in the event of fault conditions. For continuous operation, do not exceed the absolute maximum junction-temperature rating of T_J = +150°C.

Applications Information

Step-Down DC-DC Converter

Setting the Step-Down Output Voltage

Select an output voltage for BUCK1 between 0.6V and 3.3V by connecting FB1 to a resistive voltage-divider between LX1 and GND. Choose R2 (Figure 3) for a reasonable bias current in the resistive divider. A wide range of resistor values is acceptable, but a good starting point is to choose R2 as 100kΩ. Then, R1 (Figure 3) is given by:

$$R1 = R2\left(\frac{V_{OUT}}{V_{FB}} - 1\right)$$

where V_{FB} = 0.6V. For BUCK2, R3 and R4 are calculated using the same methods.

Input Capacitor

The input capacitor, C_{IN1}, reduces the current peaks drawn from the battery or input power source and reduces switching noise in the IC. The impedance of C_{IN1} at the switching frequency should be kept very low. Ceramic capacitors with X5R or X7R dielectrics are highly recommended due to their small size, low ESR, and small temperature coefficients. Due to the MAX8621Y/MAX8621Z step-down converter's fast soft-start, the input capacitance can be very low. Use a 10µF ceramic capacitor or an equivalent amount of multiple capacitors in parallel between IN1 and ground. Connect C_{IN1} as close to the IC as possible to minimize the impact of PC board trace inductance. Use a 4.7µF ceramic capacitor from IN2 to ground and a second 4.7µF ceramic capacitor from IN3 to ground.

Inductor Selection

The MAX8621Y/MAX8621Z step-down converters operate with inductors between 1µH and 4.7µH. Low-inductance values are physically smaller but require faster switching, resulting in some efficiency loss. See the *Typical Operating Characteristics* for efficiency and switching frequency vs. inductor value plots. The inductor's DC current rating needs to be only 100mA greater than the application's maximum load current because the step-down converter features zero-current overshoot during startup and load transients.

For output voltages above 2.0V, when light-load efficiency is important, the minimum recommended inductor is 2.2µH. For optimum voltage-positioning load transients, choose an inductor with DC series resistance in the 50mΩ to 150mΩ range. For higher efficiency at heavy loads (above 200mA) or minimal load regulation (but some transient overshoot), the resistance should be kept below 100mΩ. For light-load applications up to 200mA, much higher resistance is acceptable with very little impact on performance. See Table 2 for some suggested inductors.

Table 2. Suggested Inductors

MANUFACTURER	SERIES	INDUCTANCE (µH)	ESR (Ω)	CURRENT RATING (mA)	DIMENSIONS
Taiyo Yuden	CB2012	2.2 4.7	0.23 0.40	410 300	2.0 x 1.25 x 1.25 = 3.1mm^3
	LB2012	1.0 2.2	0.15 0.23	300 240	2.0 x 1.25 x 1.25 = 3.1mm^3
	LB2016	1.0 1.5 2.2 3.3	0.09 0.11 0.13 0.20	455 350 315 280	2.0 x 1.6 x 1.8 = 5.8mm^3
	LB2518	1.0 1.5 2.2 3.3	0.06 0.07 0.09 0.11	500 400 340 270	2.5 x 1.8 x 2.0 = 9mm^3
	LBC2518	1.0 1.5 2.2 3.3 4.7	0.08 0.11 0.13 0.16 0.20	775 660 600 500 430	2.5 x 1.8 x 2.0 = 9mm^3
Murata	LQH32C_53	1.0 2.2 4.7	0.06 0.10 0.15	1000 790 650	3.2 x 2.5 x 1.7 = 14mm^3
	LQM43FN	2.2 4.7	0.10 0.17	400 300	4.5 x 3.2 x 0.9 = 13mm^3
TOKO	D310F	1.5 2.2 3.3	0.13 0.17 0.19	1230 1080 1010	3.6 x 3.6 x 1.0 = 13mm^3
	D312C	1.5 2.2 2.7 3.3	0.10 0.12 0.15 0.17	1290 1140 980 900	3.6 x 3.6 x 1.2 = 16mm^3
Sumida	CDRH2D11	1.5 2.2 3.3 4.7	0.05 0.08 0.10 0.14	900 780 600 500	3.2 x 3.2 x 1.2 = 12mm^3

Dual Step-Down DC-DC Power-Management ICs for Portable Devices

Output Capacitor

The output capacitors, C7 and C9 in Figure 3, are required to keep the output voltage ripple small and to ensure regulation loop stability. C7 and C9 must have low impedance at the switching frequency. Ceramic capacitors with X5R or X7R dielectric are highly recommended due to their small size, low ESR, and small temperature coefficients. Due to the unique feedback network, the output capacitance can be very low. For most applications, a 2.2µF capacitor is sufficient. For optimum load-transient performance and very low output ripple, the output capacitor value in µF should be equal or larger than the inductor value in µH.

Feed-Forward Capacitor

The feed-forward capacitors, C_{FF} (C6 and C8 in Figure 3), set the feedback loop response, control the switching frequency, and are critical in obtaining the best efficiency possible. Choose a small ceramic X7R capacitor with value given by:

$$C6 = \frac{L1}{R1} \times 10\text{Siemens}$$

Select the closest standard value to C_{FF} as possible. For BUCK2, C8, R3, and L1 are calculated using the same methods.

LDO Output Capacitor and Regulator Stability

Connect a 4.7µF ceramic capacitor between OUT1 and ground, and a second 4.7µF ceramic capacitor between OUT2 and ground for 300mA applications. For 150mA applications, 2.2µF ceramic capacitors can be used for OUT1 and OUT2. Connect a 2.2µF ceramic capacitor between OUT3 and ground, and a second 2.2µF ceramic capacitor between OUT4 and ground. The LDO output capacitor's (C_{OUT}) equivalent series resistance (ESR) affects stability and output noise. Use output capacitors with an ESR of 0.1Ω or less to ensure stability and optimum transient response. Surface-mount ceramic capacitors have very low ESR and are commonly available in values up to 10µF. Connect $C_{OUT\_}$ as close to the IC as possible to minimize the impact of PC board trace inductance.

Thermal Considerations

The MAX8621Y/MAX8621Z total power dissipation, P_D, is estimated using the following equations:

$$P_D = P_{LOSS(BUCK1)} + P_{LOSS(BUCK2)} + P_{LOSS(OUT1)} + P_{LOSS(OUT2)} + P_{LOSS(OUT3)} + P_{LOSS(OUT4)}$$

$$P_{LOSS(BUCK1)} = P_{IN(BUCK1)} \times \left(1 - \eta/100\right) - I_{BUCK1}^2 \times R_{DC(INDUCTOR)}$$

$$P_{LOSS(BUCK2)} = P_{IN(BUCK2)} \times \left(1 - \eta/100\right) - I_{BUCK2}^2 \times R_{DC(INDUCTOR)}$$

$$P_{LOSS(OUT1)} = I_{OUT1} \times \left(V_{IN} - V_{OUT1}\right)$$

$$P_{LOSS(OUT2)} = I_{OUT2} \times \left(V_{IN} - V_{OUT2}\right)$$

$$P_{LOSS(OUT3)} = I_{OUT3} \times \left(V_{IN} - V_{OUT3}\right)$$

$$P_{LOSS(OUT4)} = I_{OUT4} \times \left(V_{IN} - V_{OUT4}\right)$$

where $P_{IN(BUCK1)}$ is the input power for BUCK1, η is the step-down converter efficiency, and $R_{DC(INDUCTOR)}$ is the inductor's DC resistance.

For example, operating with V_{IN} = 3.7V, V_{BUCK1} = 1.376V, V_{BUCK2} = 1.8V, V_{OUT1} = V_{OUT2} = 2.6V, V_{OUT3} = 1.8V, V_{OUT4} = 3V, I_{BUCK1} = I_{BUCK2} = 300mA, I_{OUT1} = I_{OUT2} = 330mA, I_{OUT3} = I_{OUT4} = 100mA, $P_{IN(BUCK1)}$ = 516mW and η = 80%, $P_{IN(BUCK2)}$ = 651mW and η = 83%:

$$P_{LOSS(OUT1)} = P_{LOSS(OUT2)} = 363\text{mW}$$

$$P_{LOSS(OUT3)} = 190\text{mW}$$

$$P_{LOSS(OUT4)} = 70\text{mW}$$

$$P_{LOSS(BUCK1)} = 94\text{mW}$$

$$P_{LOSS(BUCK2)} = 102\text{mW}$$

$$P_D = 363\text{mW} + 363\text{mW} + 190\text{mW} + 70\text{mW} + 94\text{mW} + 102\text{mW} = 1182\text{mW}$$

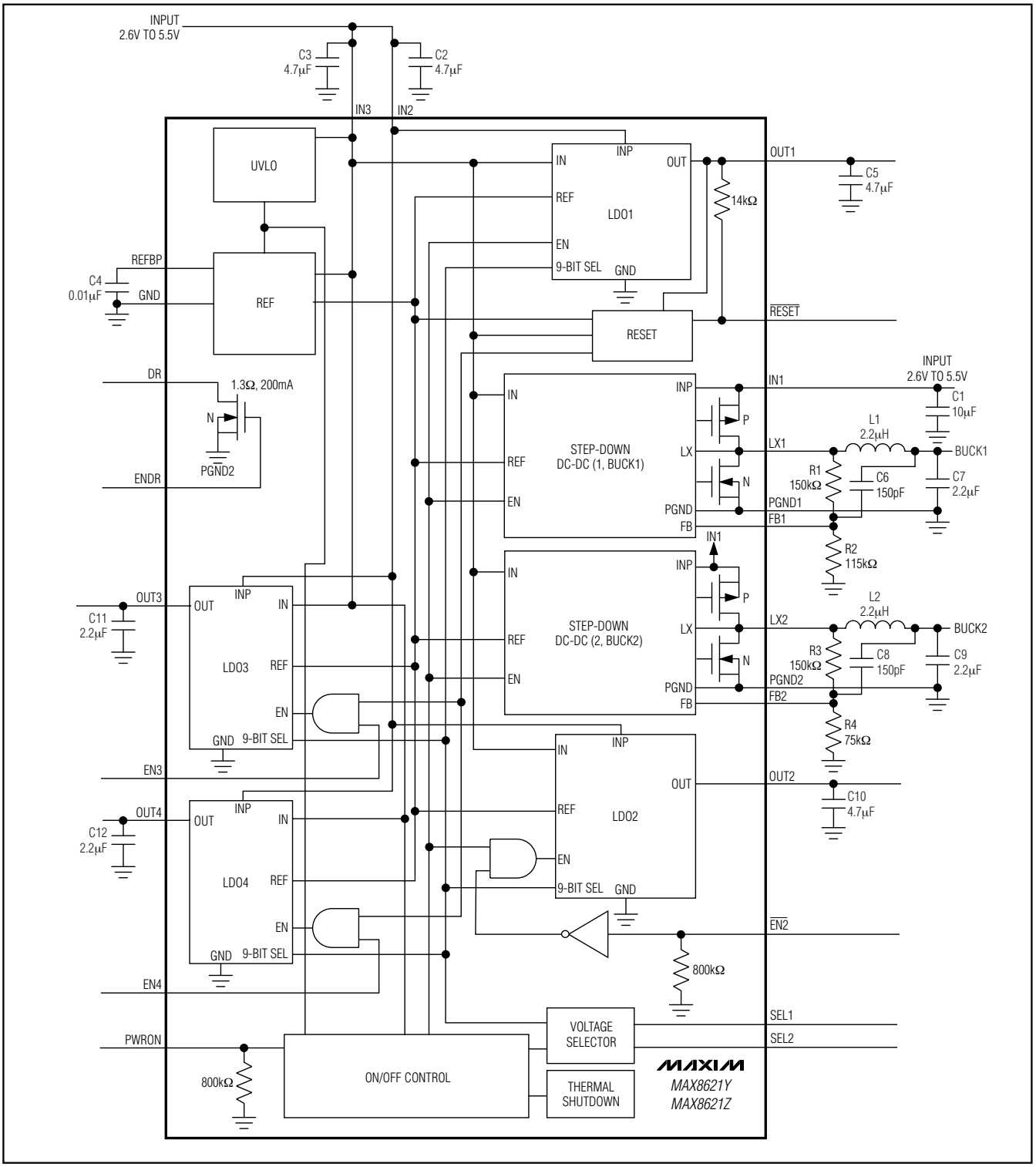


Figure 3. Functional Diagram and Typical Application Schematic

Dual Step-Down DC-DC Power-Management ICs for Portable Devices

The die junction temperature can be calculated as follows:

$$T_J = T_A + P_D \times \theta_{JA}$$

When operating at an ambient temp of +70°C under the above conditions:

$$T_J = 70°C + 1.182W\left(36\frac{°C}{W}\right) = 112.6°C$$

T_J should not exceed +150°C in normal operating conditions.

Printed Circuit Board Layout and Routing

High switching frequencies and relatively large peak currents make the PC board layout a very important aspect of design. Good design minimizes excessive EMI on the feedback paths and voltage gradients in the ground plane, both of which can result in instability or regulation errors. Connect $C_{IN\_}$ close to IN_ and GND. Connect the inductor and output capacitors ($C_{OUT\_}$) as close to the IC as possible and keep the traces short, direct, and wide.

The traces between $C_{OUT\_}$, $C_{FF\_}$, and FB_ are sensitive to inductor magnetic field interference. Route these traces between ground planes or keep the traces away from the inductors.

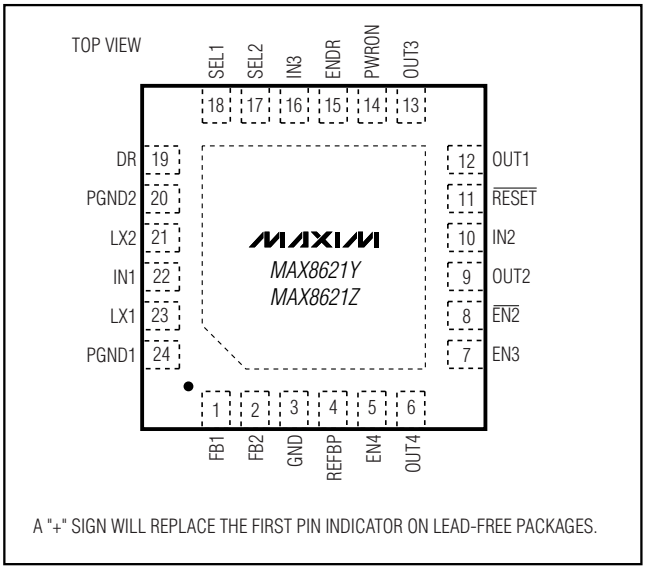
Connect GND and PGND_ to the ground plane. The external feedback network should be very close to the FB pin, within 0.2in (5mm). Keep noisy traces, such as the LX node, as short as possible. Connect GND to the exposed paddle directly under the IC. Refer to the MAX8621Y/MAX8621Z evaluation kit for an example PC board layout and routing.

Chip Information

TRANSISTOR COUNT: 5850

PROCESS: BiCMOS

Pin Configuration

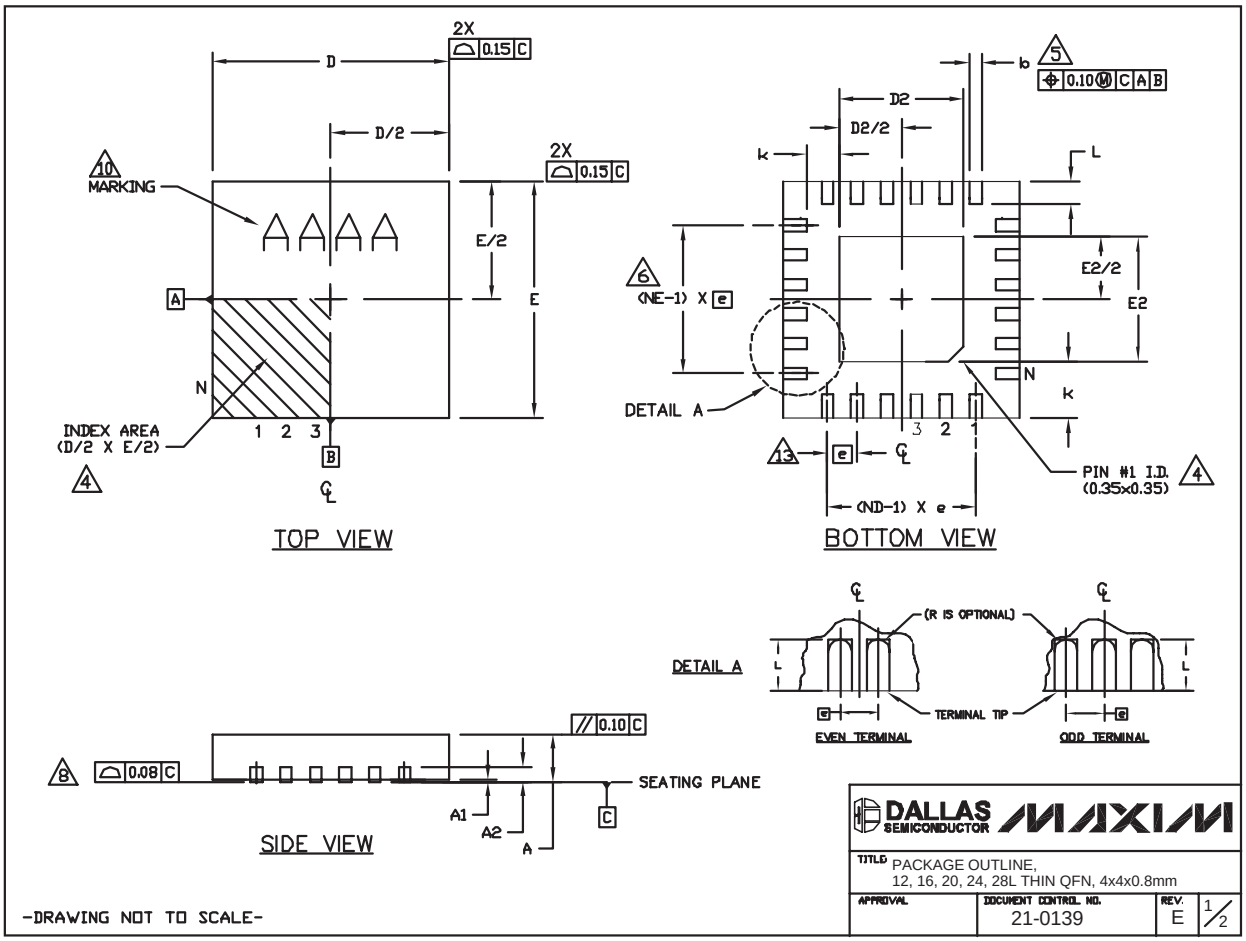


A "+" SIGN WILL REPLACE THE FIRST PIN INDICATOR ON LEAD-FREE PACKAGES.

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

24L QFN THIN.EPS



Dual Step-Down DC-DC Power-Management ICs for Portable Devices

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

COMMON DIMENSIONS															
PKG	12L 4x4			16L 4x4			20L 4x4			24L 4x4			28L 4x4		
REF.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05
A2	0.20 REF			0.20 REF			0.20 REF			0.20 REF			0.20 REF		
b	0.25	0.30	0.35	0.25	0.30	0.35	0.20	0.25	0.30	0.18	0.23	0.30	0.15	0.20	0.25
D	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10
E	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10
e	0.80 BSC.			0.65 BSC.			0.50 BSC.			0.50 BSC.			0.40 BSC.		
k	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-
L	0.45	0.55	0.65	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50	0.30	0.40	0.50
N	12			16			20			24			28		
ND	3			4			5			6			7		
NE	3			4			5			6			7		
Jedec Var.	WGGB			WGGC			WGGD-1			WGGD-2			WGGE		

EXPOSED PAD VARIATIONS							
PKG. CODES	D2			E2			DOWN BONDS ALLOWED
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
T1244-3	1.95	2.10	2.25	1.95	2.10	2.25	YES
T1244-4	1.95	2.10	2.25	1.95	2.10	2.25	NO
T1644-3	1.95	2.10	2.25	1.95	2.10	2.25	YES
T1644-4	1.95	2.10	2.25	1.95	2.10	2.25	NO
T2044-2	1.95	2.10	2.25	1.95	2.10	2.25	YES
T2044-3	1.95	2.10	2.25	1.95	2.10	2.25	NO
T2444-2	1.95	2.10	2.25	1.95	2.10	2.25	YES
T2444-3	2.45	2.60	2.63	2.45	2.60	2.63	YES
T2444-4	2.45	2.60	2.63	2.45	2.60	2.63	NO
T2844-1	2.50	2.60	2.70	2.50	2.60	2.70	NO

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220, EXCEPT FOR T2444-3, T2444-4 AND T2844-1.
10. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
11. COPLANARITY SHALL NOT EXCEED 0.08mm
12. WARPAGE SHALL NOT EXCEEND 0.10mm
13. LEAD CENTERLINES TO BE AT TRUE POSITION AS DEFINED BY BASIC DIMENSION "e", ±0.05.
14. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY

-DRAWING NOT TO SCALE-

DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE, 12, 16, 20, 24, 28L THIN QFN, 4x4x0.8mm

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0139	E	2/2